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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/025,816
Filing Date: December 26, 2001
Appellant(s): SLOBODNIK ET AL.

Stanley C. Spooner

For Appellants

EXAMINER'S ANSWER

This is in response to the appeal brief filed 02/22/2006 appealing from the Office action mailed 06/02/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellants' statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct. However, reference to prior art and arguments thereof is improper and should not be included in the summary of the claimed subject matter.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellants' statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US-5661732	Lo et al.	8-26-1997
US-6001662	Correale, Jr. et al.	12-14-1999
US-20030167428	Gold	4-13-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9, 13, 16, 17, 18-26, 30, 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Lo et al. (US-5661732) hereafter Lo.

Claims 1 and 18:

Lo teaches a ABIST micro-processor block which consists of a Micro-code Array 10, the Registers 11a-11e, and the rest of the logic known as ABIST engine 12. Lo

discloses that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes scanned-in prior to ABIST test (self-test controller configured by self-test instruction). Lo also teaches the ABIST (Array Built-In Self-Test) (self-test controller) is a small programmable micro-processor used to test and characterize on-chip arrays (at least one memory). (Col. 3, lines 61-63; col. 4, lines 28-33; FIG. 1). Lo teaches that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes (self-test instruction) scanned-in (serially loaded) prior to ABIST test. Lo further discloses these 9 bits are divided into 5 fields: three bit Pointer field 14, one bit Address Increment field 15, three bit Data Control field 16, one bit Write Control field 17, and one bit End-Of-Address-Space control field 18. (Col. 4, lines 31-37). Lo illustrates in Table 7 in Col. 10 that the value of the three bit Data Control field 16 (self-test instruction) specifies a test methodology to be applied to the memory array (i.e. WALKING, MARCHING, CHECKER_BOARD, COLUMN_STRIPE, etc.).

Claims 2 and 19:

Lo teaches that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes (plurality of self-test instructions) scanned-in prior to ABIST test. (Col. 4, lines 31-33). Lo further teaches the "sequences of memory tests" from the micro-programming examples starting in column 12, line 28 and ending column 16, line 11.

Claims 3 and 20:

Lo teaches the ABIST (Array Built-In Self-Test) 12 (self-test controller) is a small programmable micro-processor (processor) used to test and characterize (memory tests) on-chip arrays. Lo also teaches these arrays are adaptable (memory test can be changed) to state-of-the-art very/ultra large scale integration (VLSI or ULSI) chips which include the VLSI memory array elements 9 (different memories) which need to be self-tested. (Col. 3, lines 58-63).

Claims 4 and 21:

Lo teaches the programmable ABIST micro-processor block in Fig. 1 provides an improved method for testing and characterizing on-chip arrays in engineering, manufacturing, and burn-in environments (match fabrication characteristics) with programmable test patterns (different test needs), by implementing the testing of arrays with two different logical views. (Col, 3, lines 52-56).

Claims 5 and 22:

Lo teaches of a WALKING/MARCHING pattern in FIG. 5 which shows two loops. Lo further discloses that the minor or inner loop makes sure all words (rows) have done their shift and the outer or major loop ensures that shifting has been done for all bit positions (columns). (Col. 10, lines 57-60).

Claims 6 and 23:

Lo teaches the Data Pattern Generation Logic 21 receives a 3 bit Data_ cntl code, ch_abist_data.sub_ctrl(0:2), from the Micro-Code Array's field 16 to generated

various data patterns for the Array-Under-Test (self-test instruction specifies data to be written to memory). (Col. 10, lines 10-13).

Claims 7 and 24:

"...self-test controller allow one or more of the following memory test operations to be performed:

(iii) write specified data to memory locations having a checkerboard pattern of memory addresses;

(iv) read data from memory locations having a checkerboard pattern of memory addresses"

Lo teaches of the reading and writing of a checkboard pattern with the following instructions: WO_CHKB: Initialize the whole Array With ZEROs; Load dataReg with (0101...0101); Write inverted data as address advances to form CheckerBoard. Read CheckerBoard. Do the same with opposite data. (Col. 13, lines 7-10).

Claims 8 and 25:

Lo teaches the ABIST (Array Built-In Self-Test) 12 (self-test controller) is a small programmable micro-processor (processor) used to test and characterize on-chip arrays (on an integrated circuit). (Col. 3, lines 61-63).

Claims 9 and 26:

Lo teaches the memory arrays are adaptable to state-of-the-art very/ultra large scale integration (VLSI or ULSI) chips which include the VLSI memory array elements 9 (synthesized and custom memory) which need to be self-tested. (Col. 3, lines 58-60).

Claims 13 and 30:

Lo teaches data read out from the memory array also feed a bank of internal (within the array Macro) MISR registers (not shown) with feedback circuitry for signature generation (detect memory error). (Col. 4, lines 21-25).

Claims 16 and 33:

Lo teaches that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes (self-test instruction) scanned-in (serially loaded) prior to ABIST test. (Col. 4, lines 31-33).

Claims 17 and 34:

Lo teaches that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes (self-test instruction) scanned-in (external signal pin) prior to ABIST test. (Col. 4, lines 31-33).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 11,14, 27, 28 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US-5661732) in view of Gold (US-2003/0167428 A1).

Claims 10 and 27:

Lo does not explicitly teach "interface circuit serving to adapted values and timings of signals passed between said self-test controller and said at least one memory to accommodate differing value and timing properties of said at least one memory." Gold teaches a memory address converter 24 (interface circuit) converts the physical address generated by the BIST engine 20 (self-test controller) to a corresponding logical address in the embedded memory 28 (memory). (Page 2, ¶ 17). Gold suggests the address converter 24 (interface circuit) may be adapted to support built-in self-repair of the embedded memory array 28 (at least one memory). (Page 2, ¶ 21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's ABIST engine 12 (self-test controller) to couple Gold's address converter 24 (interface circuit) between Lo's next address calculation logic 20 and the memory array elements 9. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made that Gold's address converter 24 (interface circuit), in being adapted to support built-in self-repair of the embedded memory array 28 would contain the necessary circuitry to synchronize the timing of the signals connected to the memory array 28. The artisan would have been motivated to believe so because it would enable Lo's ABIST engine 12 (self-test controller) to accommodate differing value and timing properties of a memory. The artisan also, would have been motivated to believe so because built-in self-repair circuits inherently adapt the repair circuit to the memory timing it is repairing through synchronization of the signals interfacing to the

memory array. In this way the interface circuit of the instant application would already be included in Gold's address converter 24 (interface circuit).

Claims 11 and 28:

The motivation for combining Lo and Gold is per claims 10 and 27 rejection above. Gold teaches a memory address converter 24 (interface circuit) converts the physical address generated by the BIST engine 20 (address value generated by the self-test controller) to a corresponding logical address in the embedded memory 28 (memory). (Page 2, ¶ 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's ABIST engine 12 (self-test controller) to couple Gold's address converter 24 (interface circuit) between Lo's next address calculation logic 20 and the memory array elements 9. The artisan would have been motivated to do so because it would enable Lo's ABIST engine 12 (self-test controller) to access the logical addresses of the memory array elements 9.

Claims 14 and 31:

The motivation for combining Lo and Gold is per claims 10 and 27 rejection above. Lo does not explicitly teach of "a result data register included in the interface circuit". However, Lo does teach the data read out from the array also feed a bank of internal (within the array Macro) MISR registers (not shown) with feedback circuitry for signature generation. (Col. 4, lines 21-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's MISR registers to be included in Gold's memory address converter 24 (interface circuit). The artisan would have been motivated to do so because it would enable Gold's memory address

converter 24 (interface circuit), already incorporated in Lo's ABIST micro-processor block, to capture the test result data.

Claims 12, 15, 29 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US-5661732), hereafter Lo, in view of Correale, Jr. et al. (US-6001662), hereafter Correale.

Claims 12 and 29:

Lo does not explicitly teach the "specifying which memory to test via the self-test instruction". However, Lo does teach "State Machine" 24 which determines how many passes the micro-program has to be repeated for different variations of operational parameters (self-test instruction) in testing the memory array elements 9 (plurality of memories). (Col. 4, lines 46-48). Correale teaches ABIST address counter 202 is coupled to a first memory array 205, a second memory array 206 and an "Nth" memory array 208 (plurality of memories). Correale also teaches that each memory array includes a generated address mask in order to access each memory array (specifying which memory to test via the self-test instruction). (FIG. 7, Col. 6, lines 29-61). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's state machine 24 to incorporated the address masking functions of Correale's ABIST address counter 202. The artisan would have been motivated to do so because this would enable Lo to specify which to plurality of memories test.

Claims 15 and 32:

Lo does not explicitly teach the "self-test instruction specifies a size of memory to be tested". However, Lo does teach "State Machine" 24 which determines how many passes the micro-program has to be repeated for different variations of operational parameters. (Col. 4, lines 46-48). Correale teaches an ABIST controller 92 is designed to work with a variety of different sized memory arrays (specifies a size of memory to be tested). Correale further teaches ABIST state machine 122 controls the number of iterations, the incrementing and decrementing of the addresses, when to examine array compare signals, and when to switch data patterns as well as read/write controls. Correale suggests no changes to ABIST state machine 122 are necessary to test multiple arrays of different sizes. (Col. 6 lines 10-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's state machine 24 with Correale's state machine 122. The artisan would have been motivated to do so because this would enable Lo to test memories of different sizes.

(10) Response to Argument

Whether or not the Examiner has failed to properly construe the language of Appellants' independent claims 1 and 18.

The appellants argues on page 8-9, section A, that "both independent apparatus claim 1 and method claim 18 require "a self-test instruction specifying a test methodology." Each of these claims indicate that the self-test controller is responsive to such "self-test instruction specifying a test methodology"." The appellants is basing the

definition of "methodology" from the conventional definition in Webster's Ninth New Collegiate Dictionary as "a body of methods, rules, and postulates employed by a discipline: a particular procedure or set of procedures." The appellants also states, "[t]his definition is consistent with the use of the term "methodology" in the specification to mean a sequence of steps and not a single step. The remainder of the appellants' arguments in this section are based on assertion the Examiner misconstrued the meaning of "methodology", which the Examiner will show is incorrect.

To summarize Lo, the ABIST engine 12 (self-test controller) receives a 9-bit word 13 from a Microcode Array 10, which stores a set of test program codes scanned-in prior to ABIST test (self-test controller configured by self-test instruction). Lo further discloses these 9 bits are divided into 5 fields: three bit Pointer field **14**, one bit Address Increment field **15**, three bit Data Control field **16**, one bit Write Control field **17**, and one bit End-Of-Address-Space control field **18**. (Col. 4, lines 31-37).

The Examiner asserts that Lo teaches the claimed "a self-test instruction specifying a test methodology". For example, if one skilled in the art using Lo's ABIST engine 12 received a single 9-bit word (**a self-test instruction**) from the Microcode Array 10 containing a "010" in the Micro-Code Array Address Pointer field **14**, a "1" in the Address Increment field **15**, "000" in the Data Pattern Control field **16**, a "1" in the Read/Write Control Field **17**, and a "1" in the End-of –Address-Space Control field **18** from the Microcode Array 10, that is 0101000111, a test methodology (i.e. a body of methods, rules, and postulates employed by a discipline: a particular procedure or set of procedures) would be executed to set the ABIST engine 12 in write mode (Read/Write

Control Field **17,** Col. 11**,** Table 8), increment the memory address (Address Increment field **15**, Col. 10, Table 6), Shift and Rotate (Data Pattern Control field **16**, Col. 10, Table 7), detect the end of address (End-of –Address-Space Control field **18**, Col. 11**,** Table 9) and do all this repeatedly (hold the ROM pointer) until the address space has been fully explored at which time the ROM pointer is incremented to one (Micro-Code Array Address Pointer field **14**, Table 5, Col. 8). These "set of procedures" (**specifying a test methodology**) are executed as a result of **one single** 9-bit word (**a self-test instruction**) read from the microcode array 10, not from eight different 9-bit words as the appellants contend (see arguments on pages 10-11). By this the Examiner maintains the position that Lo substantially teaches the claimed invention.

Whether or not the Lo reference fails to include structures and method steps set out in properly construed independent claims 1 and 18

The appellants argue on pages 10-12, section B.1, "[t]he Lo reference fails to teach or suggest a self-test controller which is 'responsive to a self-test instruction specifying a test methodology" are fully addressed above and are not persuasive. Further, continued arguments such as "the Examiner's conclusion is incorrect. Each of the cited 9-bit microcode words teaches only a single step" on page 10; "There is no indication that a single 9-bit word can specify a sequent of test steps, i.e., a methodology" on page 11, are fully addressed above and are not persuasive.

The appellants also argue on page 11, second paragraph, "[a]ppellants have repeatedly challenged the Examiner to demonstrate how or where any microcode word

in the Lo patent teaches or defines a test methodology and the Examiner has been unable to comply with Appellants' request. In fact the discussion in Lo teaches the direct opposite, i.e., that a sequence of words is necessary to define the methodology". Even though the Examiner contends that the Appellants' request has been fully addressed in the previous Office Actions of Record, the Examiner asserts that the detailed example presented above should satisfy this request.

The appellants argue on pages 12-15, section B.2, "[t]he Lo reference fails to teach or suggest a self-test controller which may be "configured by said self-test instruction to implement different memory test methodologies"." The appellants further contend that "[t]here is no indication that the Lo reference envisions a self-test controller which in any way, shape or form could be configured by a self-test instruction "to implement different memory test methodologies". The Examiner disagrees and asserts the Lo substantially teaches that "a self-test controller may be configured by said self-test instruction to implement different memory test methodologies" as claimed. For example, Lo teaches that the ABIST micro-processor is a small programmable (configurable) micro-processor used to test and characterize on-chip arrays. (Col. 3, ll. 42-63). Among other configurable blocks in the ABIST engine 12 (part of the ABIST micro-processor), Lo teaches a State Machine 24, which determines how many passes the micro-program has to be repeated for different variations of operational parameters (**configured by said self-test instruction to implement different memory test methodologies**). (Col. 4, ll. 38-50).

Further, after careful consideration of the areas of the specification cited by the appellants (page 10, line 20 to page 11, line 16, and the table on page 21) the Examiner asserts that the argued claim limitation "said self-test controller may be configured by **a** self-test instruction to implement different memory test methodologies" (emphasis added) is not supported by the disclosure. The cited areas of the specification clearly show that one skilled in the art needs to load a different self-test instruction (pattern selection field in table on page 21) to implement a different test methodology, not a single self-test instruction to implement a [plurality of] different memory test methodologies as the appellants contend. For example, looking at the pattern selection field in table on page 21, to implement the test methodology "WriteSolids" one skilled in the art would load the pattern selection field of the self-test instruction of "0000". However, if one skilled in the art would desire to test the array with a different test methodology, say "WriteCkbd", a different pattern selection field of the self-test instruction of "0010" would have be loaded. Therefore, the Examiner asserts that present invention needs to load a different self-test instruction to implement a different test methodology rendering these arguments not persuasive.

With respect to the appellants' request to identify the self-test controller on page 15, second paragraph, the Examiner asserts that this has been identified in previous Office Actions of Record as the ABIST engine 12.

The appellants argue on pages 15-6, section B.3, "There is no basis for a rejection under 35 USC § 102". In light of the arguments presented above this argument

is rendered moot. The Examiner has met the burden to establish a proper basis for a rejection under 35 USC § 102.

Whether or not the Examiner failed to allege that the claim language missing from the Lo reference is disclosed in either the Gold or Correale references

The appellants argue on pages 16-17, section C, "[t]he Examiner has failed to allege, let alone point out where or how, either the Gold reference or the Correale reference supplies the missing claimed "self-test controller" i.e., one which is "responsive" to a self-test instruction specifying a test methodology or one which may be configured "by said self-test instruction to implement different memory test methodologies". The Examiner asserts, by the above presented arguments, that the Lo reference substantially teaches these limitations and that the Gold and Correale reference where used for the limitations of claims 10, 11,14, 27, 28 and 31 (Gold) and claims 12, 15, 29 and 32 (Correale) as presented in the grounds of rejection.

Whether or not the Examiner failed to provide any "reason" or "motivation" for combining any of the Lo, Gold and Correale references

The arguments presented by the appellants on pages 18-19, section D, first paragraph concerning motivation to combine the Lo with Gold and Lo with Correale, the Examiner asserts that the motivation and reason to combine as set forth in the Final Office Action of 06/02/2005 is proper for the following reasons.

Firstly, Lo and Gold are analogous arts. It would be obvious to one skilled in the art to combine Lo and Gold because Lo teaches an ABIST controller for testing memory arrays where as Gold teaches a BIST engine and an address converter for mapping physical addresses to logical addresses for testing memory arrays. Secondly, combining Lo and Gold clearly solves the problems in claims 10, 11,14, 27, 28 and 31 as set forth in the Final Office Action of 06/02/2005, which are "an interface circuit serving to adapted values and timings of signals passed between said self-test controller and said at least one memory to accommodate differing value and timing properties of said at least one memory" (Claims 10 and 27), converts the physical address to a logical address (Claims 11 and 28) and "a result data register included in the interface circuit" (Claims 14 and 31).

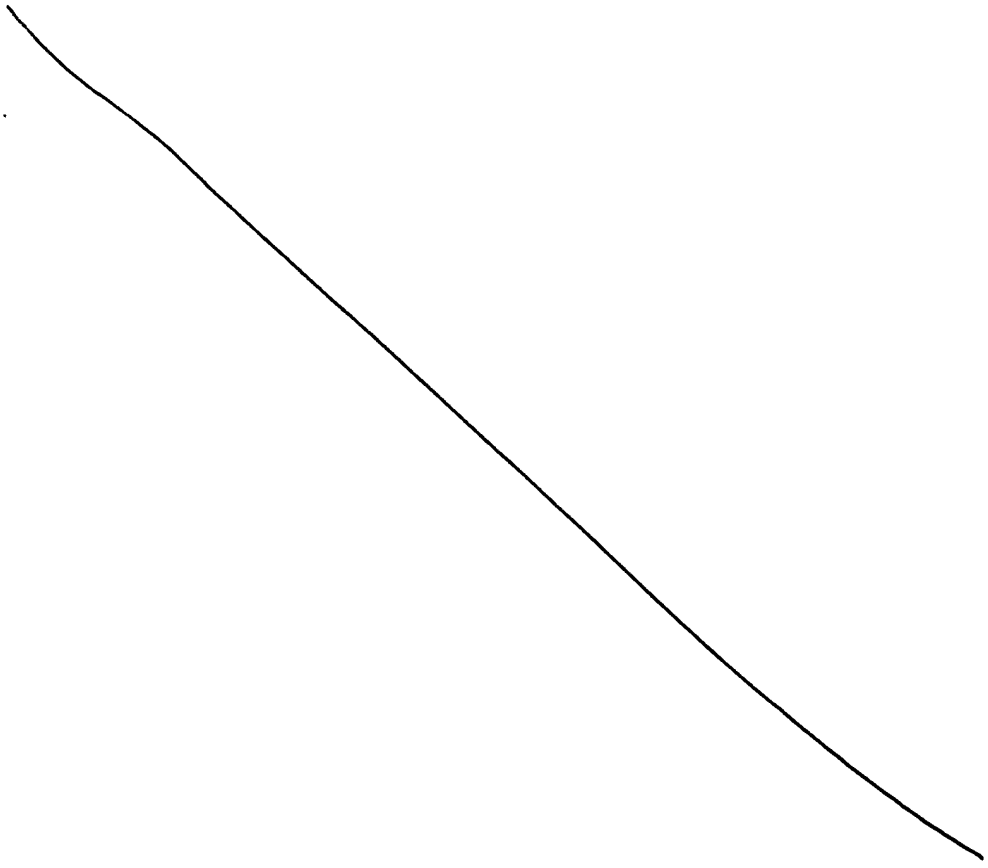
Further, the Examiner asserts that the motivation to combine the analogous arts Lo and Correale would be obvious to one skilled in the art because Lo teaches an ABIST controller for testing memory arrays where as Correale also teaches an ABIST controller that test a plurality of memories. Also, combining Lo and Correale clearly solves the problems in claims 12, 15, 29 and 32 as set forth in the Final Office Action of 06/02/2005, which are "specifying which memory to test via the self-test instruction" (Claims 12 and 29) and "self-test instruction specifies a size of memory to be tested" (Claims 15 and 32).

In response to appellants arguments presented on pages 18-19, section D, second paragraph, that the references fail to show certain features of appellants' invention, it is noted that the features upon which applicant relies (i.e., "self-test

controller" (1) which is "responsive" to a self-test instruction specifying a test methodology or (2) which may be "configured by said self-test instruction" to implement different memory test methodologies) are not recited in the rejected claim(s) (claims 10, 11,14, 27, 28 and 31 (Gold) and claims 12, 15, 29 and 32 (Correale)). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.



For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

John J. Tabone, Jr. 5/17/06

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